



Chemistry Assisted Delayering of Advanced Semiconductor Devices Using MultiChem

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Controlled deprocessing of advanced semiconductor devices requires the removal of increasingly complex stacks containing thick metallic redistribution structures, passivation layers, and densely patterned back-end-of-line (BEOL) architectures comprising alternating metal (M) and vertical interconnect access (Via) layers. Differences in material composition, layer thickness, and sputter response can lead to differential removal, surface topography, redeposition, and orientation-dependent milling artifacts, making it challenging to reproducibly stop at a selected device level while preserving the surface quality required for subsequent electrical probing and failure analysis.

Gas-assisted PFIB deprocessing allows the removal strategy to be adapted to specific materials within the semiconductor stack. Insulator Enhanced Etch (IEE) and Dielectric Etch (DE) are used to enhance dielectric removal and facilitate access to underlying metallic structures, whereas Dx chemistry is applied primarily to metallic and heterogeneous mixed-field layers. For thicker metallic or redistribution layers, where Dx-assisted delayering becomes less efficient, H₂O-assisted etching provides an alternative route for material removal.

In this work, we present a systematic and quantitative investigation of Dx-assisted PFIB deprocessing of commercially available memory and logic devices, including a 5 nm FinFET logic device (AMD Ryzen 7600), on which successive BEOL levels from V9 to M0 were exposed (see Figure 1). Surface-sensitive SEM imaging at a landing energy of 100 eV was used to visualize the exposed metal and via levels after individual delayering steps. Stable imaging at this low landing energy was enabled by automated beam-deceleration centering (ABDC), which compensates for cathode-lens misalignment and provides reproducible alignment in immersion mode using the in-column-detector [1].

Atomic force microscopy (AFM) was used to quantitatively evaluate the surface after delayering. RMS surface roughness values of 5.298 nm, 2.235 nm, and 1.466 nm were measured in logic, mixed logic/SRAM, and SRAM regions, respectively, revealing a pronounced dependence of the resulting surface topography on local device layout and material distribution. High-resolution AFM characterization of a $3 \times 3 \mu\text{m}$ SRAM region yielded an RMS surface roughness of 0.753 ± 0.066 nm, demonstrating sub-nanometer roughness within a locally homogeneous device region (see Figure 2).

These results demonstrate that chemistry-assisted PFIB processing enables controlled sequential deprocessing of heterogeneous semiconductor stacks while preserving high local surface quality. The observed dependence of surface roughness on local pattern composition further demonstrates that precursor chemistry, beam parameters, and device architecture must be considered together when developing reproducible delayering workflows for advanced semiconductor failure analysis.

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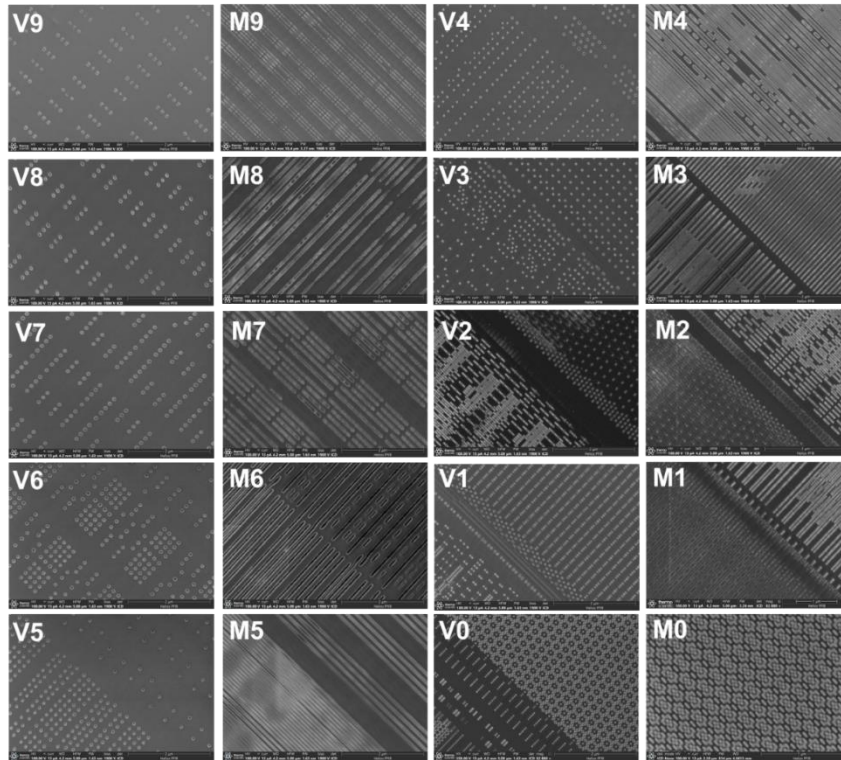


Figure 1. Layer-by-layer deprocessing of the BEOL stack (V9–M9 to V0–M0) on an AMD Ryzen 7600 device imaged at 100 V after gas assisted PFIB delayering

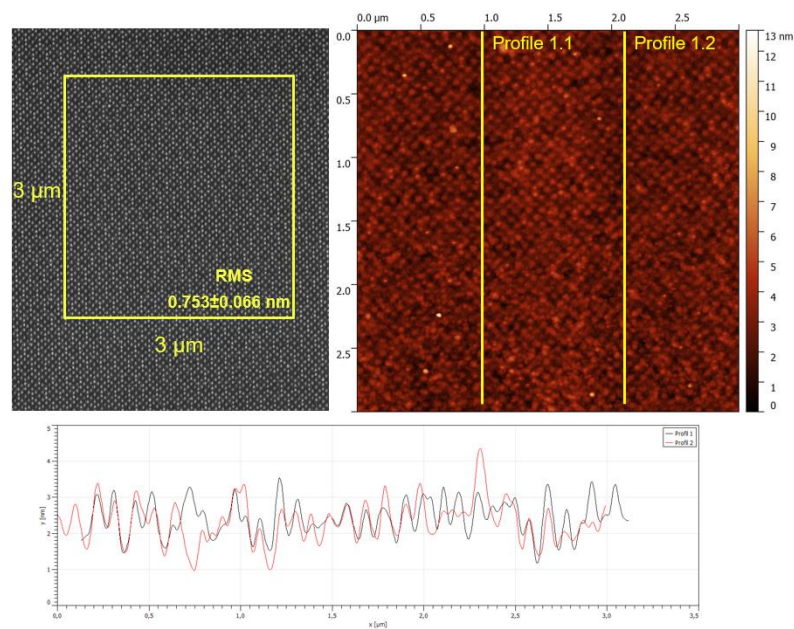


Figure 2. Nanometer Scale Surface Uniformity Confirmed by High-Resolution AFM Mapping and Height Profile Analysis.

References

- [1] Colbea, Claudiu, et al. Cathode Lens Alignment for Damage-Free Automated Device Delayering Process with Low-Energy Electron Beam. In: International Symposium for Testing and Failure Analysis. ASM International, 2025. p. 446-450.